Honeywell

4500 MBC AND MEMORY MAINTENANCE

ACPU1MEM-M

9/15/78

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4500 MBC AND MEMORY MAINTENANCE

1. INTRODUCTION

This publication provides installation, preventive maintenance, testing, troubleshooting and replacement parts information for the 4500 process computer system's Memory Bus Controller and Memory. The Memory Bus Controller is one AXMC11 board in slot 4 of the 4500 CPU chassis, and it controls the exchange of information between the memory and requestor/responders on the microprocessor bus, i.e., the Processor and GENIE Bus Controller. The MBC also contains the first 9_{10} (00_8 through 10_8) memory locations which are dedicated locations and include the index registers (01_8 through 07_8) and the Q Register (10_8). The memory consists of from one to four memory boards (from one to 11 boards in early production units) and the maximum memory size is $262{,}144_{10}$ 30-bit words (6 parity bits and 24 data bits).

2. PRECAUTIONS

The MBC and memory boards contain only logic level voltages, but to avoid damage to the logic, power must always be removed prior to removal or replacement of the boards. Because of the boards complexity they should be repaired only in the factory or an approved repair facility.

Note that if the Memory Battery Power Pack is implemented, it must also be turned off to remove power to the memory boards, prior to board removal or replacement.

WARNING

The position of the Stop on Parity Switch must be returned to its specified position prior to placing the system on-line. Failure to have the switch in its specified position may cause a process failure and thus a dangerous situation. Its position is specified in either the system documentation or locally by the proper authority.

3. OPTIONS

The MBC and 32 k* of memory are a functional requirement for the basic CPU. Additional memory is optionally available in both the CPU chassis and the optional Memory Expansion chassis. Memory boards are available in sizes of:

64 k (65,536 30-bit words) - Model AXME64**
32 k (32,768 30-bit words) - Model AXME32**

Note that only one 32 k memory board can be used per system and it must be the last 32 k of memory, as this provides continuous addresses to the top of memory. Only one 8 k board may be used in earlier CPUs.

3.1 CPU Memory Configuration

The CPU chassis may accomodate up to three memory boards - a maximum of 192 k, but if the AXMP11 memory protect board is installed, only two memory boards may be accomodated. Early production units using 16 k boards house up to 48 k in the CPU chassis. See Fig. 2.

3.2 Memory Expansion Chassis Configuration

The ACME11 Memory Expansion Chassis provides eight additional CPU slots, one or two of which can accomodate 64 k memory boards to provide the maximum 256 k memory. In early production CPUs, this chassis may accomodate up to eight 16 k memory boards to a maximum capacity of 176 k (11 16 k boards in all). If a 32 k board (or 8 k board) is used, it must be the last (highest addressed) memory board.

3.3 Mini-Switches

All four memory board types (64 k, 32 k, 16 k, 8 k) have mini-switches that must be set up for proper operation. See 9.1, 9.2 and Tables 3-1 and 3-2.

4. REFERENCES

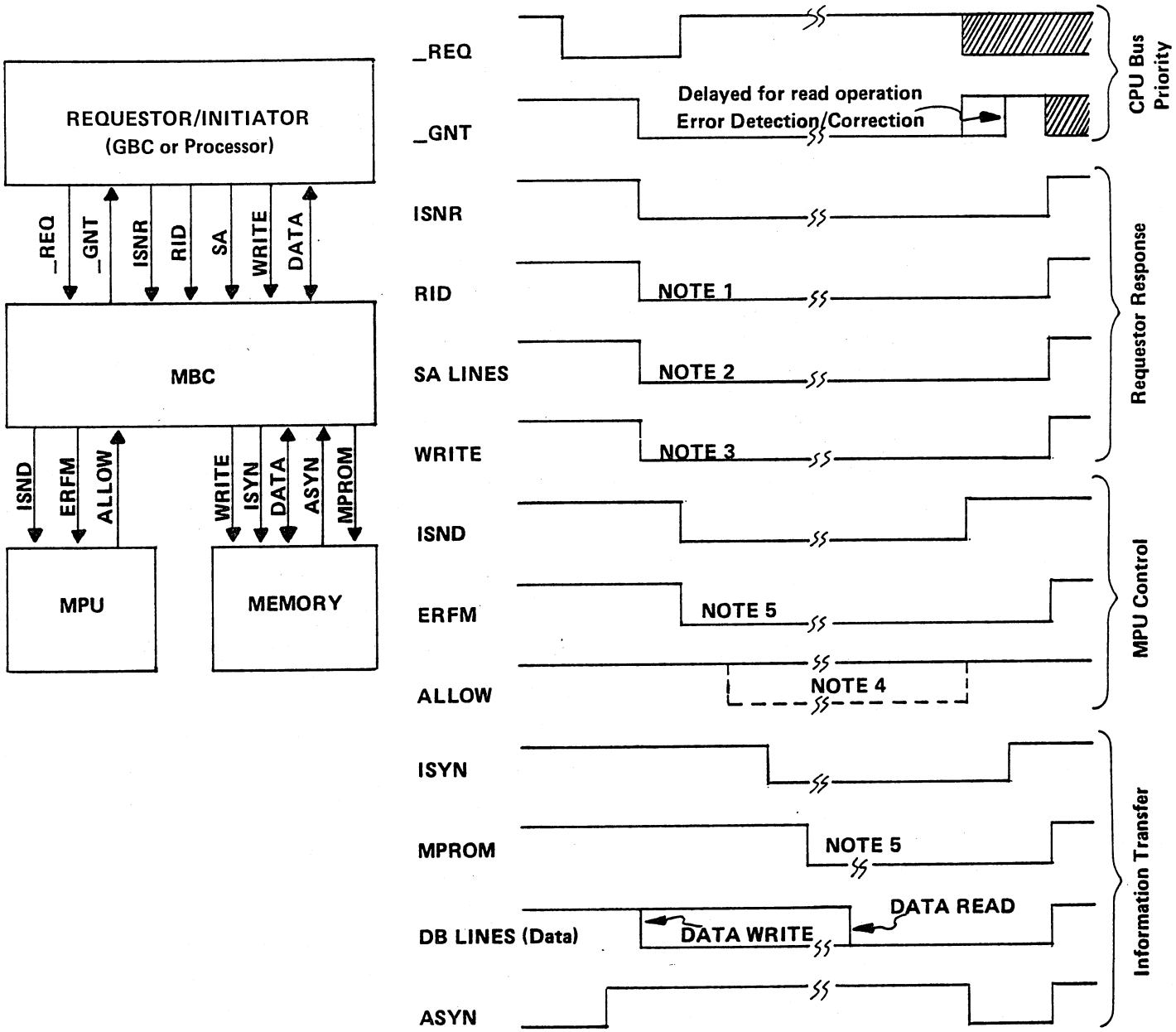
4500 CPU MBC Theory publication, number ACPU1 MEM-T, provides an overall functional description of the MBC's operation.

4500 CPU Memory Theory publication, number ACPU1-MEM-T, provides an overall description of the solid state MOS memory.

4500 Memory Test, number 51191038, which provides an operational test of both the MBC and the memory.

* Early CPU's using 16 k and 8 k memory boards must have a minimum of 16 k of memory (k = 1024_{10} words).

** Early production CPU's used AXME44 (16 k) and AXME24 (8 k).



NOTES:

1. RID lines must contain code for a memory operation.
2. SA lines must contain address of location to be accessed (10_8 or less - File Register and 11_8 or larger - memory boards).
3. Determines if operation is read or write. Write operation is indicated. Signal remains high for read operation.
4. Used only when MPU is implemented and enabled. High allows the operation and low disallows the operation to continue with the MPU returning ASYN.
5. The ERFM and MPROM signals are issued only when the File Register is being accessed.

Fig. 1 Timing Relationship, Memory Access/Cycle Operation

SIGNALS UNIQUE TO MBC		SIGNALS COMMON TO MBC & MEMORY				SIGNALS UNIQUE TO MEMORY
Priority Resolution		Address		Data		(None)
PRQ	A37	SA00	A68	DB00	A83	
GREQ	A34	SA01	A18	DB01	A33	
XREQ	A42	SA02	A67	DB02	A82	
AREQ	A92	SA03	A17	DB03	A32	
PGNT	A96	SA04	A66	DB04	A81	
GGNT	A97	SA05	A16	DB05	A31	
XGNT	B85	SA06	A65	DB06	A80	
AGNT	B30/B80	SA07	A15	DB07	A30	
LOCK	A85	SA08	A64	DB08	A79	
		SA09	A14	DB09	A29	
Control		SA10	A63	DB10	A78	
ARF	B73	SA11	A13	DB11	A28	
ERFM	B56	SA12	A62	DB12	A77	
MVLD	B45	SA13	A12	DB13	A27	
ISNR	A35	SA14	A61	DB14	A76	
ISND	B15	SA15	A11	DB15	A26	
ALLOW	B89	SA16	A60	DB16	A75	
TRAP	A86	SA17	A10	DB17	A25	
BCLR	A55			DB18	A74	
STCL	B16	RID00	A09	DB19	A24	
CHKI	A88	RID01	A58	DB20	A73	
FFP	B23	RID02	A08	DB21	A23	
				DB22	A72	
Alarm		Control		DB23	A22	
CALM	A29	MSAC	A55	DB24	A71	
ROBS	B21	ISYN	A05	DB25	A21	
		ASYN	A06	DB26	A70	
		WRITE	A07	DB27	A20	
		MPROM	A57	DB28	A69	
				DB29	A19	

Table 1 MBC/Memory/CPU Bus Interface Connections

ATPG Programs - How to Load Them, Run Them, and Use Them, publication ATPG-1, gives helpful guidance in the operation and understanding of the Memory Test and its results.

Fig. 1 provides the timing relationships required for a memory access and data transfer operation.

Table 1 provides the MBC/Memory/CPU Bus interface back-panel connections.

5. COMPONENT LOCATIONS

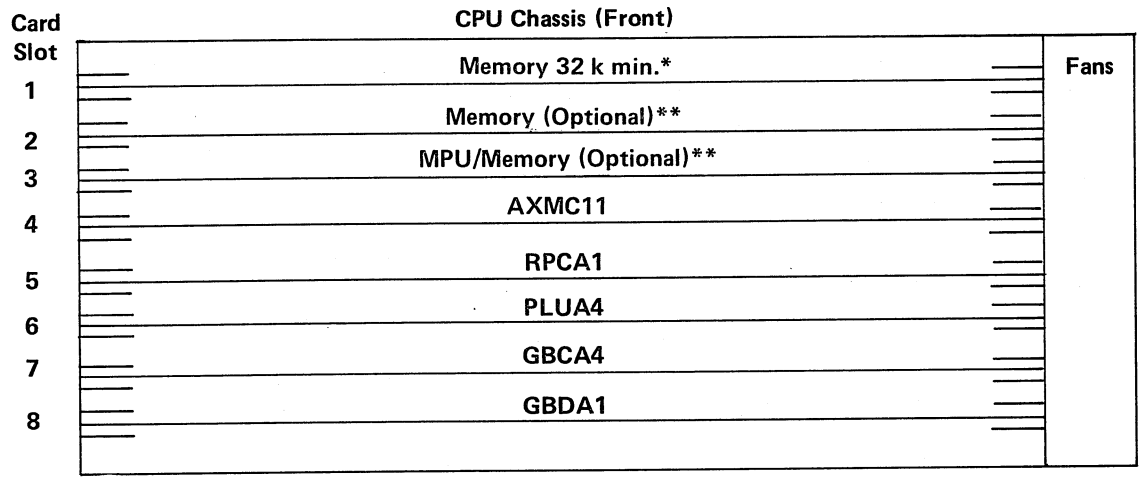
The MBC occupies one card slot in the CPU chassis with each memory board (up to a maximum of three boards) occupying one card slot each as shown in Fig. 2. Card slot 2 is presently reserved for additional memory with card slot 3 being reserved for the implementation of the MPU option or additional memory. Card slots 2 and 3 may also be used for the implementation of future options.

6. TEST EQUIPMENT AND MATERIALS

No special test equipment is required. Due to the complexity of the MBC and memory boards it is advised that the board be replaced when a problem is isolated to a particular board.

7. PREVENTIVE MAINTENANCE

Preventive maintenance is not required on the MBC or any of the memory boards.



* 16 k min. in CPUs using 16 k/8 k boards.

** These card slots may also be used for the implementation of future options.

Fig. 2 CPU Chassis Card Slot/Board Type Locations

8. PERFORMANCE TESTS

Performance of the Memory Bus Controller and memory can be verified by executing the 4500 Memory Test, 51191038. Instructions for operating the test are provided with the punched cards or tape plus reference to publication ATPG-I may provide useful. Allow the test to complete the recommended number of passes.

9. ASSEMBLY AND DISASSEMBLY

Assembly and disassembly of the MBC and memory consists only of the removal of and reinsertion of the boards. Note that when replacing a memory board with a new board requires that its address and the memory-size memory selection switches must be set like those on the removed board. Always remove power prior to removing or inserting boards.

9.1 Board Selection Address Switches

Each memory board must be set up so that only one board responds to each access. This is accomplished by setting up address switches according to the address range to be covered by each board. Each board contains 64 k or 16 k (late or early production). The physical location does not necessarily have anything to do with the address range covered, but, normally, the lowest addresses are in the lowest physical memory slots and the highest addresses are in the highest slot. Table 3-1 shows how the address switches are set up on the 64 k/32 k boards and Table 3-2 shows the set up on 16 k/8 k boards.

9.2 Memory Present Switches

AXME32 boards (32 k); AXME44 boards (16 k) at revisions A, B, and C; and AXME24 boards (8 k) at revisions A and B; all have "memory present" selection switches that must be set up to allow or block a response by a board. If a board does have memory in the range addressed, response is allowed. If it does not, the response is blocked. Of course, the AXME64 board and the AXME44 board have full complements of memory ICs (chips) so they are allowed to respond to all addresses within their range. AXME32 boards and AXME24 boards are "depopulated" and should not respond to addresses in the second half of their address range. Instructions for setting up these switches are on Table 3-1 and the top half of Table 3-2. Later revisions of the AXME44 and AXME24 have the selection hardwired and do not require such switch set ups.

10. ADJUSTMENTS

There are no adjustments related to the MBC and it is recommended that no adjustments be attempted on the memory boards. The memory timing is set at the factory and if a timing problem should arise, it is recommended that the board be returned to the factory for repair and/or re-timing.

11. TROUBLESHOOTING

This section provides general troubleshooting information to isolate faults to a specific memory board or to the MBC.

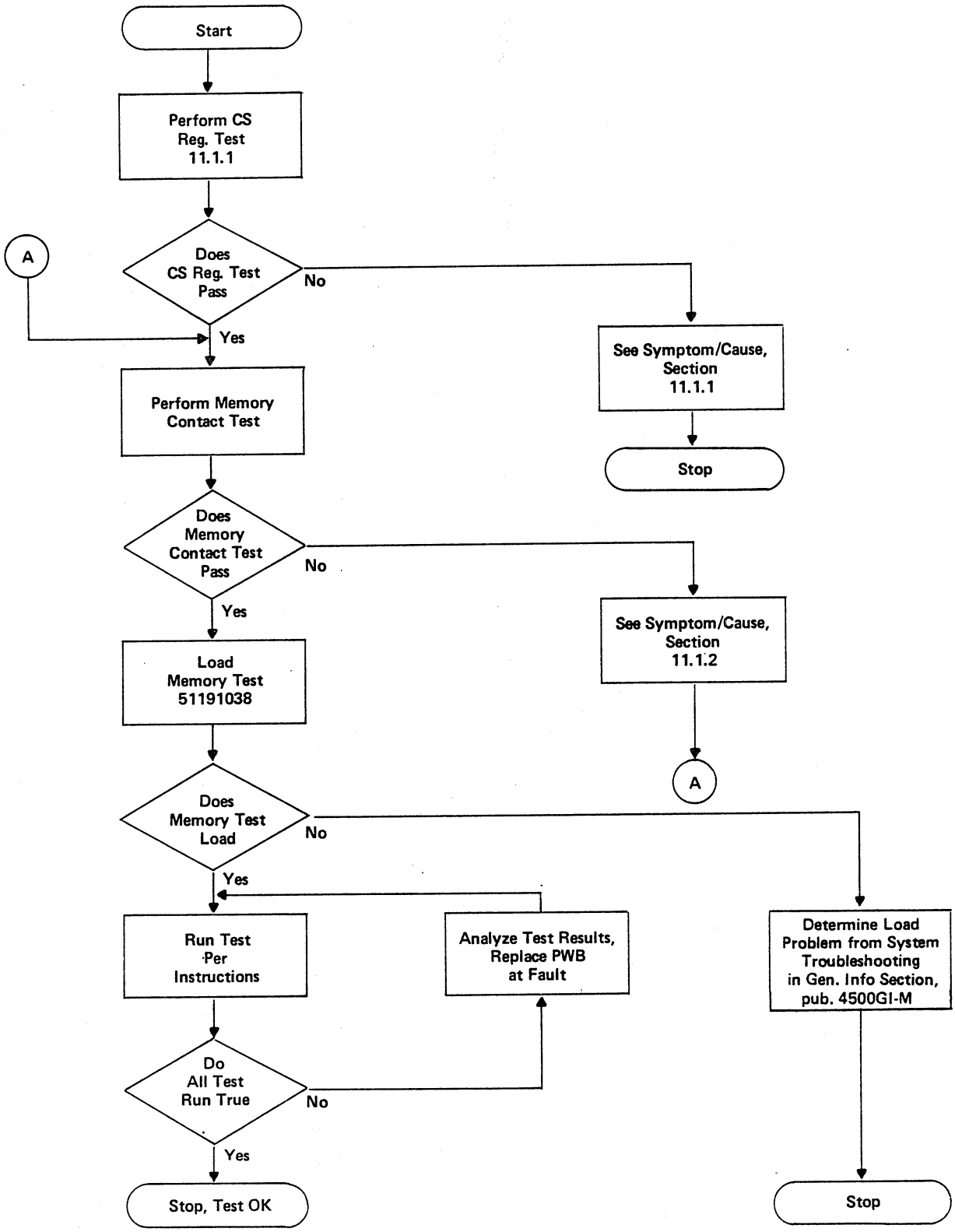


Fig. 3 Troubleshooting Flowchart

The MBC and memory boards are not considered repairable by field maintenance personnel. Therefore replacement of suspected boards will be the primary tool for isolation of failed boards. The following procedures should prove helpful in identifying the suspected boards.

11.1 Console/Memory Interaction Tests

These tests establish basic communication between the Programming and Maintenance Console, the Memory Bus Controller, and Memory. These tests provide information about the interaction between the MBC and memory and about solid failures within the MBC or memory.

11.1.1 CS Register Test

This test checks the interaction between the console, GENIE* Bus, GENIE Bus Controller, PALU, CPU Bus, and the MBC.

1. Apply power. Place console Panel Security switch in Enabled position. Press the RESET and Keypad 0 pushbutton to initialize the hardware.

2. The CS Register should be selected, this is indicated by the illumination of the CS MONITOR indicators on the console panel.

3. Enter data (other than all zeros) into the CS Register (See Console Theory or Maintenance publications for procedures on console operation).

4. Select any of the other registers and verify that the data displayed for that register is different from what was entered into the CS Register.

5. Select the CS Register again and verify that the data in the CS Register is still the same as what was entered in step 3.

SYMPTOMS: (Note that the symptom numbers correspond to the probable cause numbers.)

1. Console indicator and display do not light on power up.

2. After the Reset operation, one or all of the following are not as described:

   CS indicator is lit (CS Register is selected).

   Display contains data (data is undefined at this time).

   HALT indicator is lit (Halt mode is selected).

   S/LO indicator is lit (Stall Alarms are locked out).

   I/LO indicator is lit (Interrupts are locked out).

   ALM indicator is <u>not</u> lit (if lit it indicates an alarm condition still exists after a GENIE clear and system clear).

3. Cannot enter data into the CS Register (display does not change).

4. Content entered does not remain displayed when EXEC is pressed on data entry.

5. Content in CS Register is different from that which was entered upon return from another register.

PROBABLE CAUSE: (Note that the probable cause numbers correspond to the symptom numbers.)

1. No power is being applied to the console. Refer to the CPU Power Subsystem Maintenance publication ACPU1PS-M for troubleshooting guidance.

2. The GBC or PALU is not properly executing the Reset operation; the console is failing to initiate the Reset operation or a console indicator failure; or the GBC not returning the proper indicator coding to light the indicators. Refer to the Console Maintenance document, ACPU1CON-M and/or to the GBC/PALU Maintenance publications, ACPU1GBC-M and ACPU1ALU-M.

3. Failure of the GBC, PALU, or Console logic. Refer to the Console Maintenance, ACPU1CON-M, and/or GBC/PALU Maintenance, ACPU1GBC-M and ACPU1ALU-M.

4. Failure of the MBC or PALU, contents were lost while attempting to store in the CS Register (location 17_8 of the File Register in the MBC).

5. Failure of the MBC, contents were lost while attempting to retrieve from the CS Register (loss of all contents may indicate the PALU or GBC while loss of one or two bits more likely indicate the MBC). Note that the data retrieved from the File Register is not parity checked.

For symptoms 4 and 5 replace the MBC board with the known good board and attempt to re-run this test. If this does not correct the problem refer to the Console and GBC/PALU Maintenance publications for guidance.

*Trademark

Memory Accessed	Console Entry Data							
	23 22 21	20 19 18	17 16 15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
MBC R.F.		0	0	0	0	0	0 / 1	x / 0
1st 64 k	0	0	0 - 1	x	x	x	1 - 7	1 - 7
2nd 64 k	0	0	2 - 3	x	x	x	x	x
3rd 64 k	0	0	4 - 5	x	x	x	x	x
4th 64 k	0	0	6 - 7	x	x	x	x	x

Note 1

Note 2

Note 3

Notes:

1. Addresses 0_8 to 10_8 address the MBC Register File. Adresses 11_8 and up address the memory boards.

2. Memory boards are selected by bits 16, and 17.

3. "x" can be any number between 0 and 7. Bits 0 through 14 address the specific memory location.

Table 2-1 Board Location/Addresses, 64 k/32 k Boards

Memory Accessed		Console Entry Data							
		23	20	17	14	11	8	5	2
		22	19	16	13	10	7	4	1
		21	18	15	12	9	6	3	0
	MBC R.F.	0	0	0	0	0	0	0/1	x/0
	1st 16 k	0	0	0	0-3	x	x	1-7	1-7
	2nd 16 k	0	0	0	4-7	x	x	x	x
	3rd 16 k	0	0	1	0-3	x	x	x	x
	4th 16 k	0	0	1	4-7	x	x	x	x
	5th 16 k	0	0	2	0-3	x	x	x	x
	6th 16 k	0	0	2	4-7	x	x	x	x
	7th 16 k	0	0	3	0-3	x	x	x	x
	8th 16 k	0	0	3	4-7	x	x	x	x
	9th 16 k	0	0	4	0-3	x	x	x	x
	10th 16 k	0	0	4	4-7	x	x	x	x
	11th 16 k	0	0	5	0-3	x	x	x	x

Note 1

Note 2

Note 3

Notes:

1. Addresses 0_8 to 10_8 address the MBC Register File. Adresses 11_8 and up address the memory boards.

2. Memory boards are selected by bits 14, 15, 16, and 17.

3. "x" can be any number between 0 and 7. Bits 0 through 13 address the specific memory location.

Table 2-2 Board Location/Address, 16 k/8 k Boards

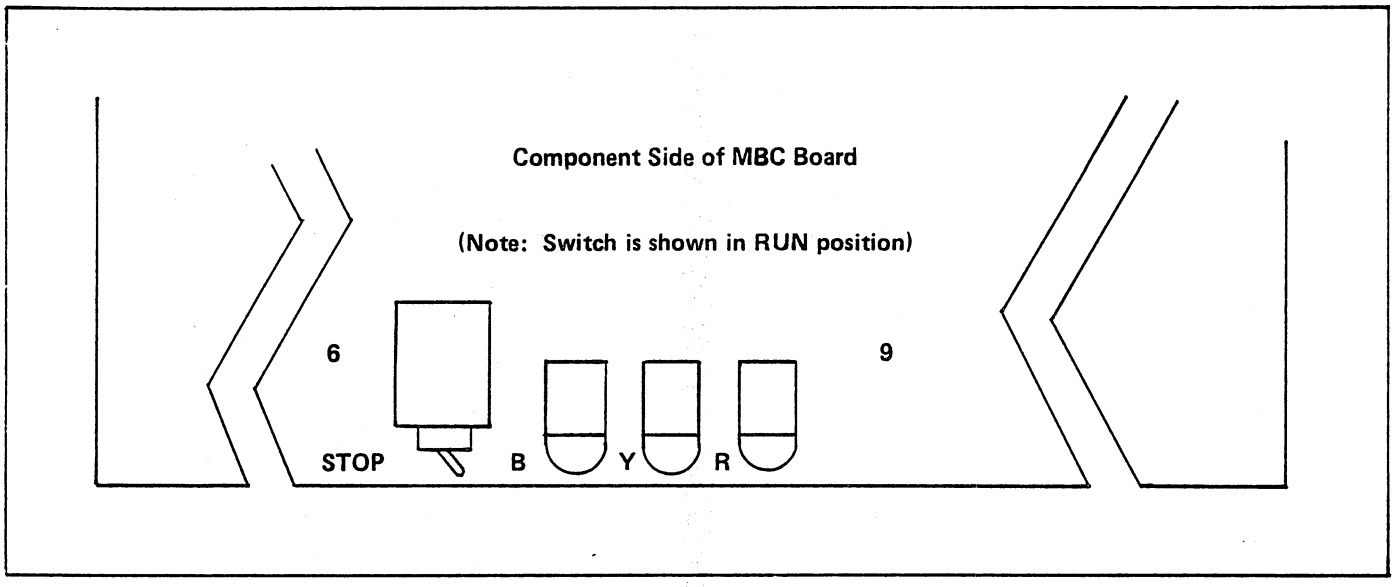


Fig. 4 MBC Rear Edge Illustration

11.1.2 Memory Contact Test

This test is performed after the CS Register test is completed satisfactorily. Its purpose is to establish basic console to memory communication with each of the memory boards.

1. While still in the Enabled position, Halt mode, with the Stall Lockout and Interrupt Lockout enabled, select the memory address for one of the Register File locations (see Table 2-1 or 2-2 for the required board address). Enter data (any random number desired except all ones or zeros) into that location (record the data). Observe that the data remains displayed as entered after the EXEC pushbutton is pressed.

2. Select another Register File location and enter data (a different random number) into that location (record the data). Observe that the data remains displayed after the EXEC pushbutton is pressed.

3. Return to the previous location (step 1) and verify that the data is still present as entered.

4. Perform steps 1 through 4 for two or more locations on each of the memory boards implemented.

SYMPTOMS: (Note that the symptom numbers correspond to the probable cause numbers.)

1. Cannot enter data into the Register File location addressed (0_8 to 10_8).

2. Cannot enter data into the memory board location addressed (11_8 and up).

3. Contents entered do not remain displayed when EXEC is pressed on data entry.

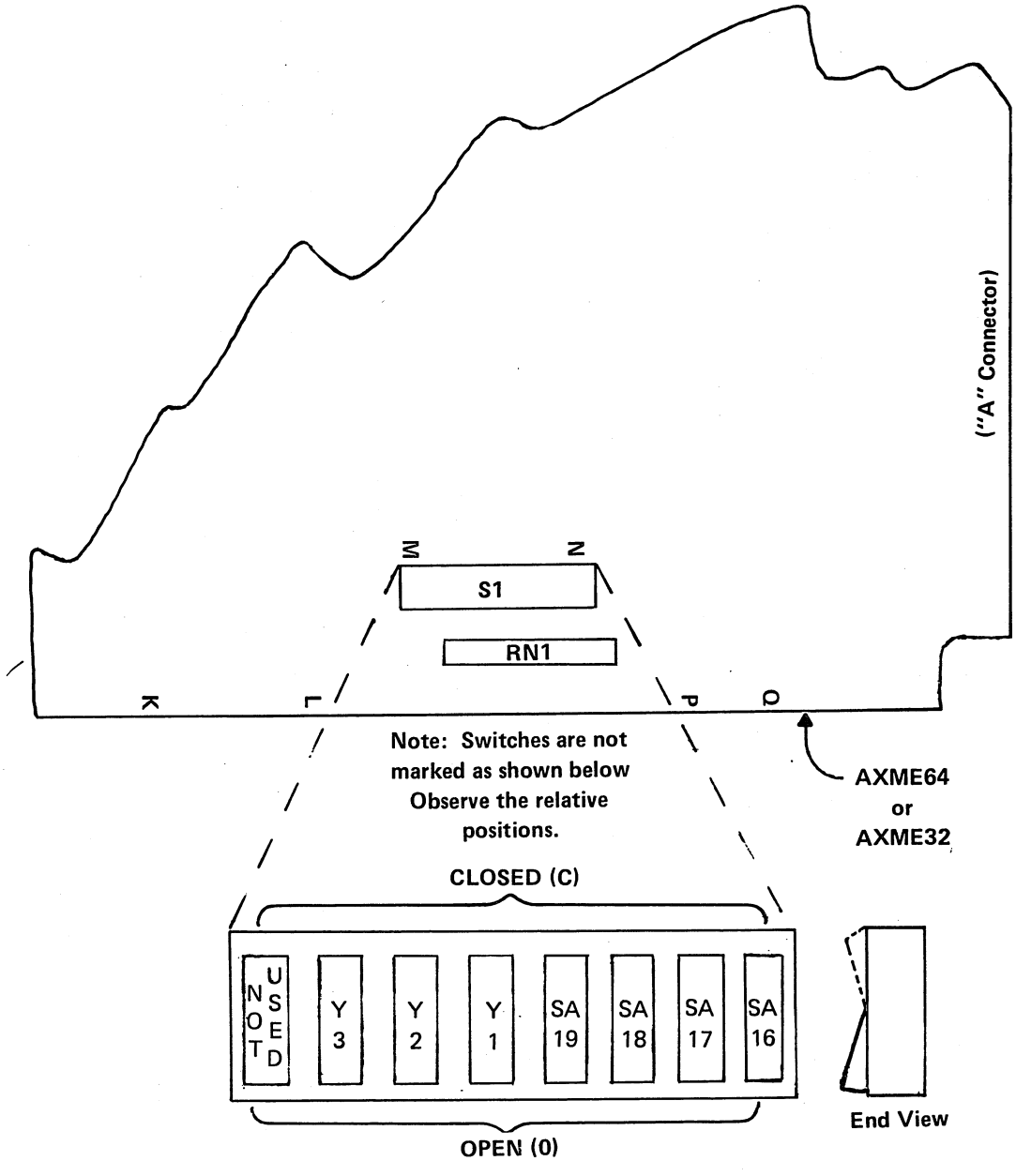
PROBABLE CAUSE: (Note that the probable cause numbers correspond to the symptom numbers.)

1. Failure of the MBC. Replace MBC with known good MBC and attempt test again. If failure still exists check for GBC failure.

2. a. (All boards and all locations fail.) Failure of the MBC, CPU Bus, MPU if implemented, or a memory board. Check Blue error status indicator on MBC, if lit, indicates a handshaking problem.

   b. (One or more but not all boards fail.) Failure of the memory board(s) where test failure occurred.

3. Failure of the MBC or memory. Contents were lost while attempting to store them in memory.



	SA19	SA18	SA17	SA16	Range
1st Board	C	C	C	C	O→(64 k - 1)
2nd Board	C	C	C	0	64 k→(128 k - 1)
3rd Board	C	C	0	C	128 k→(192 k - 1)
4th Board	C	C	0	0	192 k→(256 k - 1)

Y1, Y2, and Y3 are all normally closed. The only exception is on AXME32 (32 k) where Y2 and Y3 should be open and Y1 should be closed. Y2 and Y3 open signal "Memory Not Present" if the upper 32 k, not on the board, is addressed.

Table 3-1 Board Addressing and Memory Present Switches, 64 k and 32 k Boards

11.2 Memory Test

The TDC 4500 Memory Test, 51191038, was developed by the Automatic Test Program Generator (ATPG) program and provides the capability to check each location in memory a multitude of times per each test.

The Memory Test provides the following tests of the memory. The MBC and parts of the PALU and GBC are tested by the operation/execution of the Memory Test.

TEST 0 PRE TEST

PURPOSE - To set up memory map and trap for unknown parity

TEST 1 TEST ERROR DETECTION AND CORRECTION

PURPOSE - To check the ability of the hardware to detect and correct single bit errors and to detect double bit errors

TEST 2 ADDRESS UNIQUENESS TEST

PURPOSE - To check every address from top of program to end of memory using the address and its complement as data and checking each entry twice for cross talk.

TEST 3 MAINTENANCE AID-WRITE DATA

PURPOSE - To write hand loaded parameter into locations specified.

TEST 4 MAINTENANCE AID-WRITE ADDRESS

PURPOSE - To write addresses into locations specified.

TEST 5 MAINTENANCE AID-WRITE ADDRESS COMPLEMENT

PURPOSE - To write complement of addresses into locations specified.

TEST 6 MAINTENANCE AID-READ

PURPOSE - To read from memory addresses as specified.

12. PARTS

The MBC and memory boards are considered non-repairable in the field, therefore, they are the replaceable parts.

Memory Bus Controller	-	4DP3AXMC11
Memory (16 k)	-	4DP3AAXME444
Memory (8 k)	-	4DP3AAXME244
Memory Expansion Chassis	-	4DP3AACME110

Most error conditions will result in a message typeout. This typeout when analyzed will usually provide an indication of the memory address where the error occurred, thus an indication of the board which requires replacement.

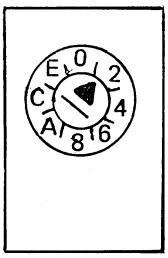
Follow the instructions provided with the Memory Test. It may also be helpful to consult publication ATPG-I for guidance in the operation and understanding of the Memory Test and its results.

ADDRESS BITS 17 16 15 14	MEMORY BOARD	SWITCH POSITION
0 0 0 0	1st = 16k	0
0 0 0 1	2nd = 32k	1 (')
0 0 1 0	3rd = 48k	2
0 0 1 1	4th = 64k	3 (-)
0 1 0 0	5th = 80k	4
0 1 0 1	6th = 96k	5 (.)
0 1 1 0	7th = 112k	6
0 1 1 1	8th = 128k	7 (,)
1 0 0 0	9th = 144k	8
1 0 0 1	10th = 160k	9 (/)
1 0 1 0	11th = 176k	A
1 0 1 1	12th = 192k	B (/)
1 1 0 0	13th = 208k	C
1 1 0 1	14th = 224k	D (\)
1 1 1 0	15th = 240k	E
1 1 1 1	16th = 256k	F (\)

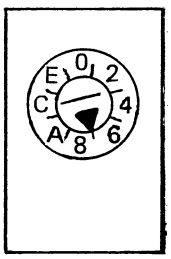
ADDRESS SELECT SWITCH POSITIONS
(AXME24 and AXME44 rev. "A" thru "E")

MEMORY PRESENT SELECTION	SWITCH POSITION
8k	1 (')
16k	7 (,)

MEMORY PRESENT SELECT SWITCH POSITIONS
(AXME24 rev. "A" and "B" and
AXME44 rev. "A", "B", and "C")*



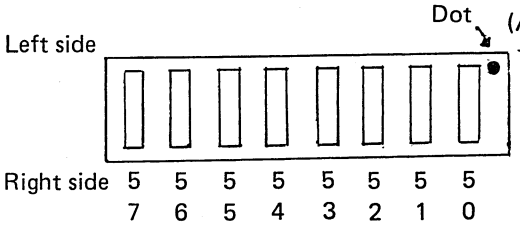
ADDRESS SWITCH
Location L16



MEMORY SELECT
SWITCH Location
G10

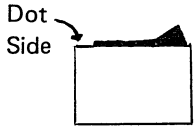
* Not required on later revisions.

ADDRESS BITS 17 16 15 14	MEMORY BOARD	SWITCH POSITION S7 S6 S5 S4 S3 S2 S1 S0	OCTAL SETTING EQUIVALENT
0 0 0 0	1st = 16k	1 0 0 1 1 0 0 1	231
0 0 0 1	2nd = 32k	1 0 0 1 1 0 1 0	232
0 0 1 0	3rd = 48k	1 0 0 1 0 1 0 1	225
0 0 1 1	4th = 64k	1 0 0 1 0 1 1 0	226
0 1 0 0	5th = 80k	1 0 1 0 1 0 0 1	251
0 1 0 1	6th = 96k	1 0 1 0 1 0 1 0	252
0 1 1 0	7th = 112k	1 0 1 0 0 1 0 1	245
0 1 1 1	8th = 128k	1 0 1 0 0 1 1 0	246
1 0 0 0	9th = 144k	0 1 0 1 1 0 0 1	131
1 0 0 1	10th = 160k	0 1 0 1 1 0 1 0	132
1 0 1 0	11th = 176k	0 1 0 1 0 1 0 1	125
1 0 1 1	12th = 192k	0 1 0 1 0 1 1 0	126
1 1 0 0	13th = 208k	0 1 1 0 1 0 0 1	151
1 1 0 1	14th = 224k	0 1 1 0 1 0 1 0	152
1 1 1 0	15th = 240k	0 1 1 0 0 1 0 1	145
1 1 1 1	16th = 256k	0 1 1 0 0 1 1 0	146



ADDRESS SWITCH
Location L16

ADDRESS SELECT SWITCH POSITIONS
(AXME24 and AXME44 rev. "F" and later)



(End View of Switch Pack)

"0" = SW, Down Left as shown

"1" = SW, Down Right.

Table 3-2 Address Selection/Memory Present Selection, 16 k and 8 k Boards

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